Datasheet

*Pro*Vision

Highly-automated Boundary-scan Application Development Software

- **Creates board tests, system tests and programs devices**
- **Multi-board systems with multiple netlist import**
- **Built-in high-precision fault coverage analysis tool**
- **Built-in application executive (AEX Manager)**

Background

JTAG Technologies BV designs and develops a comprehensive line of hardware and software products to test electronics printed circuit board assemblies (PCBAs) and program devices mounted on PCBAs using the JTAG/Boundary-scan interface (IEEE Std.1149.1) and related standards.

Their tools are used widely in manufacturing plants world-wide and also within leading electronics R&D centres - providing superior test access to complex, high-density PCBAs.

*Pro*Vision Features

- Easy-to-learn, easy-to-use platform for rapid preparation of all JTAG/boundary-scan test and in-system programming applications with user language options (English, French, German, Portuguese, Chinese, Japanese)
- Highly automated development tools handle non-boundary-scan devices via an extensive model library
- Project Database builder imports netlist (from EDA tools) and BOM data as required
- Built-in Python language scripting feature (JTAG Functional Test) for bespoke cluster tests
- Supports board-level, system-level and board-to-board testing
- Flash programming including blank-check, read-ID, erase, program and verify for NAND and NOR and serial (SPI, I2C) flash devices
- PLD programming support for all industry formats, SVF, JEDEC, JAM, STAPL, IEEE 1532
- Universal and concurrent programming of CPLDs from multiple vendors
- Advanced testing and programming through MCU debug modes (aka CoreCommander processor emulation test)
- Automatic generation of tests and diagnostics for advanced digital networks based on IEEE 1149.6
- Integrated testability analysis of maximum theoretical fault coverage and actual achieved level

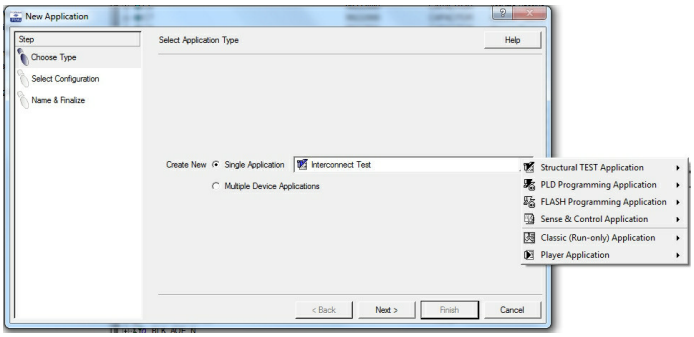
Introduction

JTAG ProVision is a comprehensive, professional-level, application and project development system for preparation of both JTAG/boundary-scan tests and in-system device (IC) programming applications. ProVision is highly automated, utilising a library of thousands of device models to rapidly generate structural tests, functional tests and IC programming routines. All the generated applications can be optimized, validated, and run within the ProVision environment prior to delivery of complete unit under test (UUT) test and programming sequences to the manufacturing/testing facility.

Advanced features include a precise test coverage analysis tool and optionally Visualizer circuit schematic and PCBA layout viewers. These tools enable the engineer to rapidly assess the thoroughness of the generated tests and to make improvements prior to release.

Project-Focused Tool Suite for Developers

JTAG *Pro*Vision, delivers genuine ease of use while maintaining the need for a high-performance, high-quality development tool. Since *Pro*Vision requires only minimal boundary-scan knowledge and basic design information/data, it speeds-up application generation allowing engineers to focus on the testability of their designs. Models for tens of thousands of different non-boundary-scan devices allow JTAG *Pro*Vision to automatically control signals on the target board for optimum, safe, test coverage and ISP performance. *Pro*Vision's project-orientated approach supports various levels of



UUT complexity, from a single board to multi-board systems, in line with the needs of all enterprises. From those handling just a few prototypes each year to large organisations with many ongoing projects. Completed projects can be archived for porting between development platforms or to any runtime environment such as those installed at a contracted manufacturing location. The design wizard guides users intuitively requiring no prior knowledge of the boundary-scan protocol.

Managing Your Design

The foundation of JTAG *Pro*Vision is the project database, consisting of the relevant design information (Netlists, BOMs BSDL files and models for non-boundary-scan devices) required for your boundary-scan applications. Built-in utilities allow you to explore and manage the project information database, view the results, and generate boundary-scan applications.

Netlists, imported from the board design environment, describe the connectivity of your board and device type details. Alternatively create a no-netlist project using the smart 'chain scanner' tool.

A bill of materials (BOM) can also be imported, an important feature if you wish to specify parts not placed on specified versions of your board or when you wish to direct the model search to your own part references.

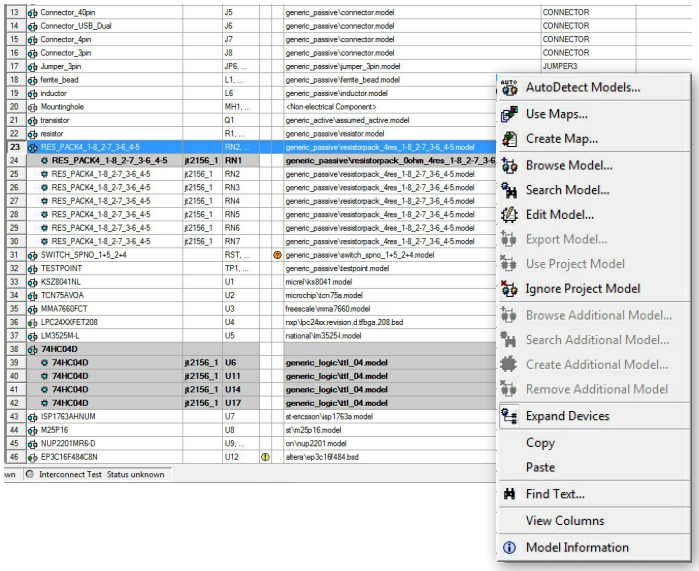
BSDL files and Device Models

IEEE 1149.1 (1993 => 2013), 1149.6 and 1532 BSDL files describe the topology and function of the boundary-scan components in your design. When a new device is added to the project database, the corresponding BSDL file from the device manufacturer is automatically checked for syntactic accuracy. JTAG *Pro*Vision includes an extensive library of models for non-boundary-scan devices including passives, generic logic and (flash) memories. Models provide control information for automatic enabling and disabling an individual device to ensure safe testing (of interconnects and logic clusters) and in-system programming. In many cases models also include test vector data to allow automatic cluster test generation or device programming - without coding. The device library is expanded regularly with over 30 000 device families now included, covering more than 260 000 devices.

Device Type Manager

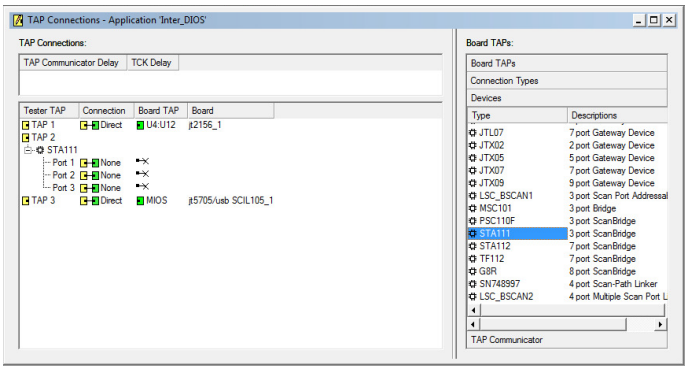
The device types extracted from CAD/EDA netlists are associated with either BSDL model files or models from *Pro*Vision's extensive component library.

A mapping file can be created that preserves the design instance ⇔ model type relation. Mapping files can be re-used saving time in future development projects while 'Search' and 'Auto-detect' features quickly assign models to new design device types. Individual device instances can be mapped to their own model file (down to an application level) in the case that customised or programmed devices change their behaviour e.g. configured FPGAs.



Multi-board UUTs

Easily generate multi-board assembly applications using JTAG *Pro*Vision's Board Connection Editor. This feature supports graphical definition and editing of connections between the target boards that comprise and assembly (e.g. mother/daughter cards) and/or auxiliary IO modules known as DIOS (digital IO scan). Additionally the TAP Connection Editor allows users the flexibility to rearrange TAP ordering and to introduce ScanBridge and Gateway infrastructure devices to create advanced TAP infrastructures using simple 'drag and drop' techniques.

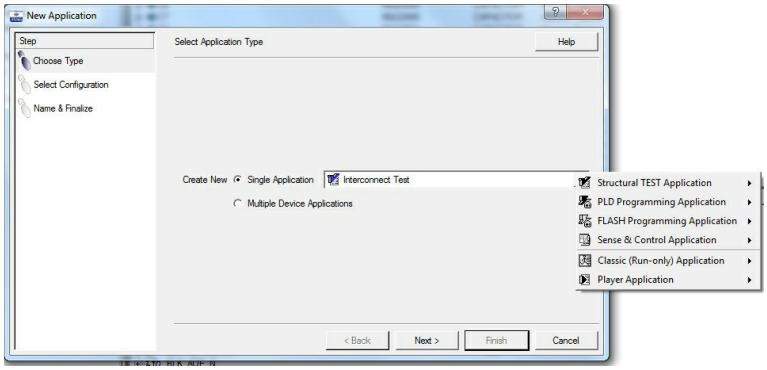


Application Level Configurations

Within each project the individual applications can be configured with their own set of 'variables' which can include: the number of target boards; the number of fixed drive or sense nets; net connections, device operating modes e.g. BYPASS, HIGHZ Functional etc. as well as bespoke device model mapping.

Process Flow

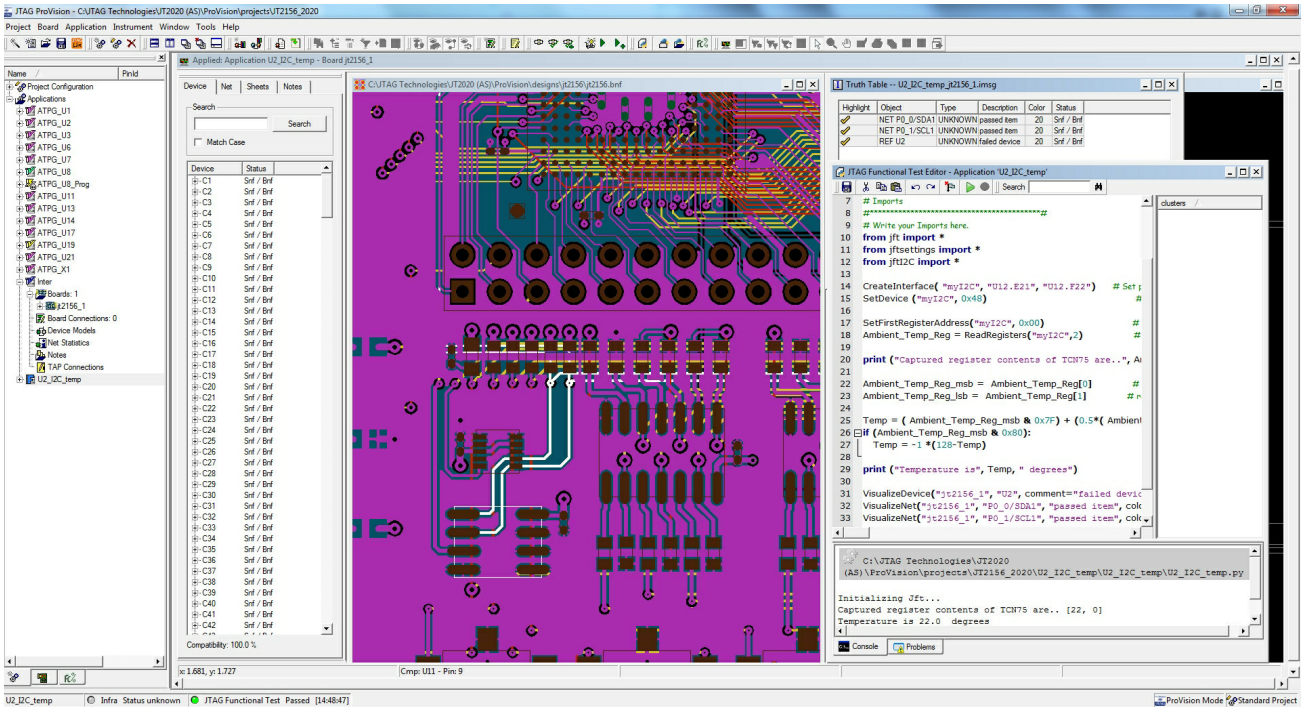
JTAG *Pro*Vision's wizard guides the development process using the same graphical interface for both test and programming applications. An applications tab provides an index of the various tests and programming routines as they are developed. A 'Test All' feature helps you generate a full set of applications including: boundary-scan infrastructure, interconnections, memories, logic clusters, and dot6, all automatically. Application execution is via one of JTAG Technologies controller range. Which can interface via USB, E-net, FireWire, PCI(e) or PXI(e).



Test Results Display

Following structural test execution results are presented in a detailed truth table reporter (TTR) display screen, with net and pin details available by simply "hovering" the mouse. Within TTR you can also display nets attached to an individual part or set your own selection of nets to simplify your data view. Boundary-scan Diagnostics (BSD) further interpret the results and indicate the probable failure cause(s), down to the pin level in most cases, even for IEEE 1149.6 test failures. Reports from both TTR and BSD can also be displayed as 'overlays' in Visualizer schematic and layout viewers.

Finally a sequencing tool opens the Application Executive (AEX Manager) and allows you to create sequences of your tests and programming applications to run in the production environment. AEX Manager can store print or export sequence reports as part of the process.

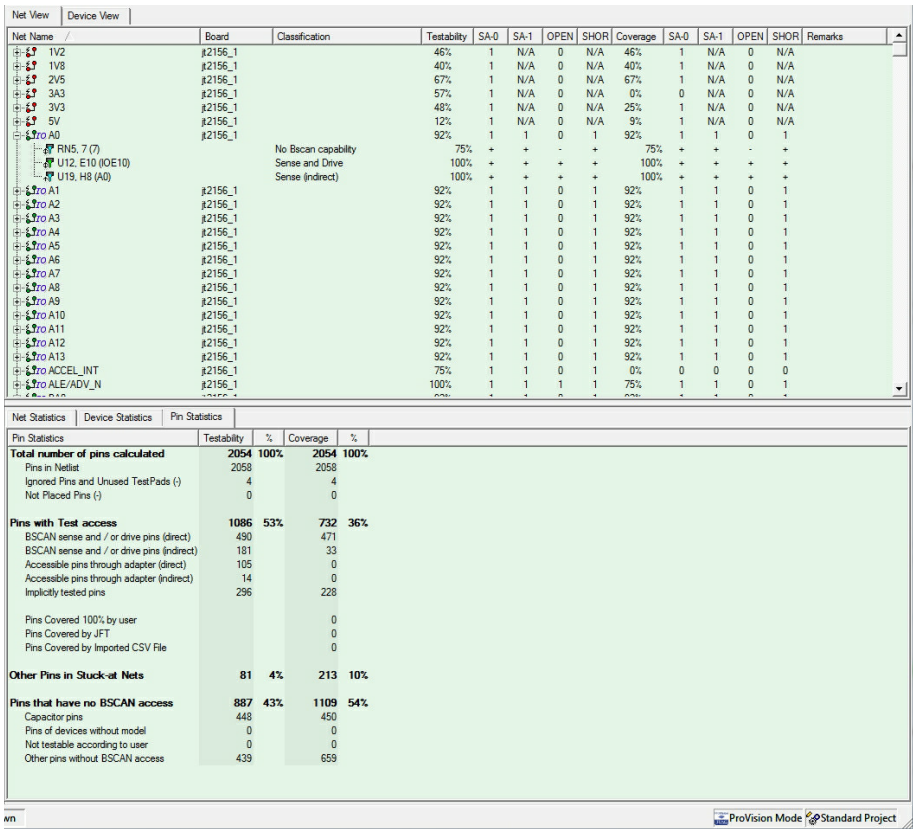


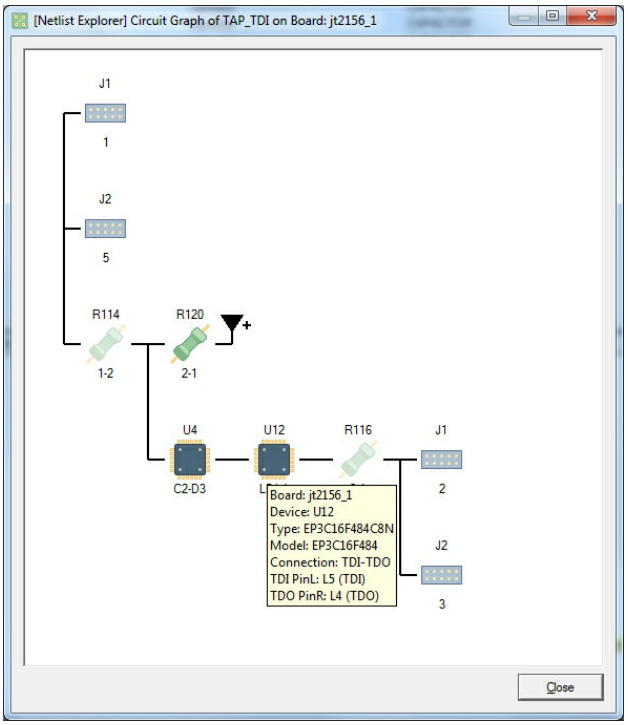
Datasheet

Fault Coverage Analysis

Assessment for fault coverage is possible from the earliest stage of project definition. From just a design netlist *Pro*Vision's examiner can estimate 'testability' by assigning boundary-scan capability to individual ICs. Adding models for the boundary-scan devices (BSDLs) and operational models for the remaining parts improves the accuracy of the report further. Finally, after tests have been developed, an actual coverage figure is produced which offers precise values for test effectiveness at pin-level, net level or device level. A percentage testability figure is based on the ability of a test to check against four key metrics: I) open circuit, II) short-circuit, III) stuck-at one and IV) stuck at zero.

Pin coverage figures feed into net coverage figures which produces an aggregate score for that net. Coverage reports can be exported in CSV or HTML formats and can also be overlaid onto Visualizer display graphics.





Python-based JTAG Functional Test

One of *Pro*Vision's most powerful and flexible features is a built in API that utilizes the popular Python programming language to create flexible, bespoke applications using JFT and associated libraries.

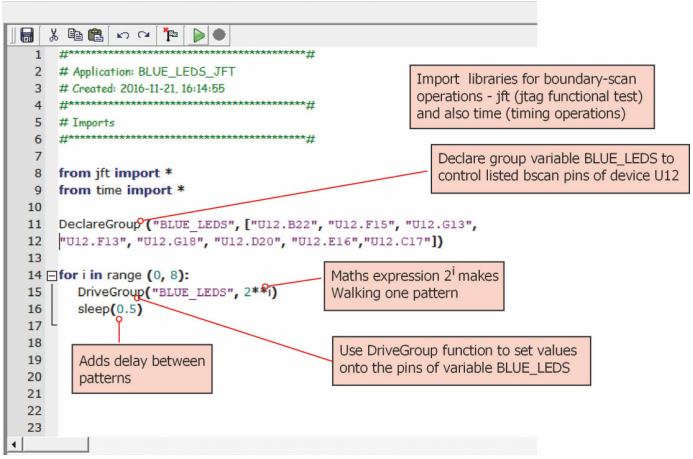
With Python/JFT it is easy to create tests with user input, conditional branching and variable handling - making it ideal for taking analog measurements, performing limits testing and managing 'loop on error' type procedures.

Exciting Novel Features

From our patented Circuit Graph to Buzz and WatchPlus, *Pro*Vision is loaded with test and debug aids that allow you to analyse your design and stimulate pins through the power of boundary-scan. Trace circuit connections from net to net with Circuit Graph, activated via NetExplorer, TTR or a BSD diagnostics report and get clear connectivity details.

Use WatchPlus to monitor pin activity (uses JTAG SAMPLE mode) in a tabular format or with Visualizer to see graphically pin states on your board layout. Buzz out individual connections using Circuit Graph and Visualizer schematics and layout.

Our PDF viewer allows user to load up schematics in the *Pro*Vision environment and search for net and pin names to aid development and debug.



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MIOS & DAF support

Mixed-signal IO Systems, and Digital Analog Frequency systems are hardware test modules developed by JTAG Technologies to support enhanced testing using the following signal processing capabilities:

- Frequency measure;
- Analog measure (single-ended and differential;
- Analog source (single ended or differential);
- Pulse generator, and
- Interval timer.

The functions are supported by dedicated MIOS/DAF GUIs included in *Pro*Vision and also by libraries supplied as part of *Pro*Vision's Python/JFT system.

Core-Commander (µP support)

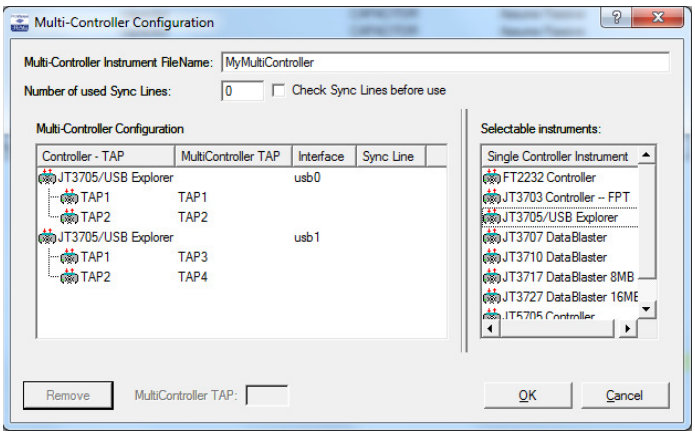
Optional core-commander modules offer a unique capability to access µprocessor cores (or a FPGA gateway) to create tests from a device's kernel. By utilising the 'emulation mode' of many popular device cores, such as ARM Cortex, PowerPC, TI C2000, etc. Users can get access to the embedded IP modules within a device, this can then allow advanced testing via DDR controllers, ADC & DACs, and comms modules for I2C or E-net, etc.

Cross-compatibility

*Pro*Vision can be switched into a 'JTAGLive' mode that offer the same look and feel as the acclaimed low-cost JTAG Live tools suite that offers access to Buzz, AutoBuzz, WatchPlus, Script and Clip testfeatures. Projects can also be saved into the JTL (project) and JLA (archive) file formats.

Custom Multi-controller

For demanding applications that require the features of more than one JTAG controller - users can create their own custom virtual controller by combining the facilities of available hardware into one synchronised system. For example combine three JT 37x7 controllers to create a mammoth 12 TAP controller/programmer.



*Pro*Vision Modules Ordering Information

*Pro*Vision has been built using a modular approach allowing users to configure the most appropriate system to suit their needs and budgets. Options are available for full developer systems /A or those targeted to simply Test, Flash ISP or PLD ISP (known as 'Stations'). Run-time only full or targeted systems are known as 'Platforms'. These Stations and Platforms can be identified in the table below from their suffix and are available with node-locked or floating licenses.

	ProVision GUI	Application Compilation	Netlist Explorer	AEX Sequencer-Reporter	JFT/Python Execution	TTR-Net-level Diagnostics	Test Execution	Flash ISP Execution	PLD ISP Execution	Model Library/Editor	APG Test Appplications	API for JFT/Python	Fault Coverage Examine	APG Flash (NOR, NAND)	APG PLD (SVF, JED,1532)	BSD - Diagnostics	CoreCommander	Visualizer Viewers
ProV_PL/T	✓	✓	✓	✓	✓	✓	✓									○	○	○
ProV_PL/F	✓	✓	✓	✓				✓										
ProV_PL/P	✓	✓	✓	✓					✓									
ProV_PL/A	✓	✓	✓	✓	✓	✓	✓	✓	✓							○	○	○
ProV_TST	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓			○	○	○
ProV_FST	✓	✓	✓	✓				✓		✓				✓				
ProV_PST	✓	✓	✓	✓					✓	✓					✓			
ProV_AST	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	○	○	○

Global Representation

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