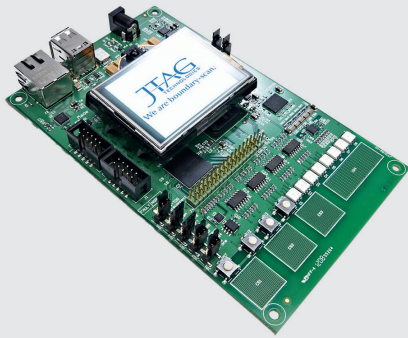


# JT 2156 Training Board

Devised to demonstrate all the latest features and test techniques available



- ✓ **Effective training target**
- ✓ **Includes typical modern device types**
- ✓ **ARM 7TDMI Core NXP processor**
- ✓ **Touch screen controller**

While previous JTAG/boundary-scan (IEEE Std. 1149.1) training and demonstration designs have been adequate in teaching the basic principles and simple test modes such as boundary-scan interconnection, they have not always been representative of modern designs. The JT 2156, however, features a host of current, widely used BGA and other SMT packaged devices that allow access to more abstract JTAG/boundary-scan - orientated tests and programming applications. In this way the JT 2156 can be used to learn more advanced techniques beyond the basic principles and simple test modes.

## Training courses

*ProVision* and *JTAGLive* both feature built-in HTML 'training sites' based around the JT 2156 that offer a step-by-step guide to building all types of test and programming applications. Advanced on-site developer's training courses based on JT 2156 can be requested via [info@jtag.com](mailto:info@jtag.com).

## Global Representation

Want to know more about our solutions and products?  
Please contact us at our head office or visit our contact page.

### JTAG Technologies (Headquarters)

Boschdijk 50, 5612 AN Eindhoven, The Netherlands  
+31 (0)40 295 0870  
[info@jtag.com](mailto:info@jtag.com)  
[www.jtag.com](http://www.jtag.com)

### 'Standard' test and ISP applications

Standard test and ISP application that can be run on the JT 2156 include:

- i) Scan path infrastructure (includes BSR length);
- ii) Bscan pin to bscan pin interconnect test;
- iii) DDR memory cluster testing;
- iv) LED illuminations;
- v) Clock toggle-check tests;
- vi) USB controller cluster test
- vii) Resistor pull-up/down presence checks; and
- viii) Direct FPGA programming.

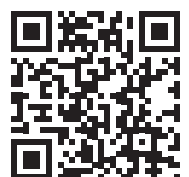
### 'Enhanced' test and ISP applications

Enhanced JTAG orientated applications, many of which are handled by JTAG Technologies' powerful Python-based scripting module JFT (JTAG Functional Test) include:

- i) Various tests through I2C and SPI bus emulation in JFT
- ii) Serial PROM programming using Altera's Active Serial mode;
- iii) Testing of the Ethernet PHY;
- iv) Analog value capture and limits testing
- v) Tests activated through our CoreCommander processor core debug access option, such as real-time PWM, ADC, DDR testing, I2C etc.

Use the QR code for an overview of our global offices and local representatives:

[www.jtag.com/contact-us](http://www.jtag.com/contact-us)



We *are* boundary-scan.®