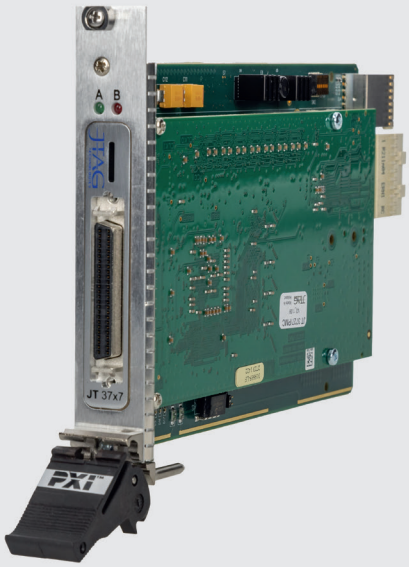
Datasheet

JT 37x7/PXIe JTAG/boundary-scan controller

The highest speed and fastest throughput of the JTAG range



- **40 MHz TCK**
- **4 TAPs**
- **External QuadPod**
- **PXIe slot**

Introduction

The JT 37x7/PXIe is member of the 'DataBlaster' category of boundary-scan controllers and offers the highest speed and fastest throughput of the JTAG range. All variants of the JT 37x7 are both scalable (in terms of local memory) and are configured for a variety of interfaces. The JT37x7/PXIe version is designed for the plug-in slots of a PXI chassis.

The unit is supplied complete with a robust bench-top signal conditioning module known as 'QuadPod' (JT 2147) that connects to the main unit via a high-density, shielded 50-way cable assembly.

The QuadPod assembly supplied comprises of a JT 2148 transceiver module plus four removable JT 2149 TAP pods as standard. Each JT 2149 features a 20-way TAP connector that also includes ports for flash memory AutoWrite, Ready/Busy and other application specific signals. A further eight pin connector provides four static IO lines per pod – suitable for PSU switching or device mode selection (eg EMU/JTAG). JT 2149s can also be remotely sited using an optional one meter extender cable without affecting the performance of the system.

Special functions, analog and frequency

Individual JT 2149s can be replaced with alternative function units that include: JT 2149/ DAF that allows Digital, Analog and Frequency measure capabilities; JT 2149/(e)MPV a TAP module that also includes 32 channels of DIOS* – JTAG synchronized DIO; plus a further range of SCIL (scan configured interface logic) modules that provide support for other bus interfaces such as NXP/Freescale's BDM or MicroChip ICSP, etc.

** Digital IO Scan – allows UUT tests to be enhanced with synchronized IO that can connect to connectors or test points on your UUT.*

High reliability pod options

In addition to the standard desktop pod type the JT 37x7/PXIe can be paired with a number of other variants generally used within bespoke ATE systems. These units have JT 2148 and JT 2149 features built onto a single PCBA and are packaged into specialized form factors as follows:

JT 2147/BO – Break-Out version for generic test systems – all TAP signals, static IO lines, optional DIOS channels and optional SCIL functions are available through vertical mounted IDC connectors

JT 2147/eDAK – MAC Panel enhanced Direct Access Kit version mainly (but not exclusively) for use with PXI controllers built into a MAC Panel 'Scout' mass interconnect receiver system – all TAP signals, static IO lines, optional DIOS channels and optional SCIL functions are available through MAC Panel 200 pin connector

JT 2147/VPC – Virginia Panel Corporation version mainly (but not exclusively) for use with PXI controllers built into a VPC mass interconnect receiver system – all TAP signals, static IO lines, 64 DIOS channels and optional SCIL functions are available through VPC 192 pin 'Quadrapaddle' connector

Performance options

In order to meet the high throughput demand of factory testing and device programming by JTAG, JT 37x7/PXIe DataBlasters can run boundary-scan application code in an optimized binary file format known as BSX. In this way the units can maintain high-speed execution of up to 40 MHz TCK – fast enough to handle all PCBs and devices currently available. The architecture of JTAG Technologies hardware and software products permits applications to be easily ported between development and production, regardless of the controller types.

The three DataBlaster configuration option levels are:

- ***JT 3707*** — base-level model suitable for board testing, CPLD programming and flash programming of small data blocks in engineering environments. This model can be upgraded to the higher performance JT 3717 for the cost difference plus service charge
- ***JT 3717*** — mid-range suitable for all applications including in-system programming of CPLDs and flash memories via the built-in 64 Mbit FIFO buffer store it is suitable for board test in manufacturing (low and high volume) and debugging environments.
- ***JT 3727*** — suitable for all applications including in-system programming of CPLDs and flash memories via the built-in 128 Mbit FIFO buffer store it is suitable for board test in manufacturing (medium and high volume), legacy applications and debugging environments.

Instrument variant	JT 3707/PXIe	JT 3717/PXIe	JT 3727/PXIe
Number of TAPs	4	4	4
TCK Range (internal source)	1 kHz - 40 MHz	1 kHz - 40 MHz	1 kHz - 40 MHz
Output Voltage Range	1.0 V - 3.6 V	1.0 V - 3.6 V	1.0 V - 3.6 V
Input voltage threshold	0.6 V - 1.8 V	0.6 V - 1.8 V	0.6 V - 1.8 V
Number of DIO	16 (4 per TAP)	16 (4 per TAP)	16 (4 per TAP)
Interal FIFO buffer (flash image)	0 Mbits	64 Mbits	128 Mbits
Interfaces Supported	PXIe	PXIe	PXIe

Global Representation

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