

# SCIP - Serial Controlled IC Programming

Solutions for programming  $\mu$ Processors,  $\mu$ Controllers, DSPs with embedded flash



## Key features

- Multiple busses and protocols supported (JTAG, BDM, Microchip, SPI, I2C) using JTAG SCIL modules where required.
- In-system program (ISP) technique minimises device handling and reduces static and mechanical damage
- Re-use existing JTAG hardware (JT 37x7) for both ISP and testing.
- Reduced fixture complexity and costs as a result of reduced hardware considerations

Although many devices have standardised on JTAG (IEEE Std 1149.1) for programming and testing circuit assemblies there is no unified standard for the way internal or embedded flash memories are programmed. The use of 'private' JTAG instructions and sometimes non-standard logic means that most regular JTAG/boundary-scan toolsets cannot support the variety of devices that now use JTAG or variants as their programming interface.

Furthermore there is a secondary class of devices that use other, often lower pin count, interfaces to support their programming examples of the alternative interfaces are BDM, SPI, Serial Wire Debug, etc..

JTAG Technologies SCIP family offers a range of options that can be used by engineers to improve their device programming facilities without adding much in the way of additional hardware. To accommodate the various device types and their unique requirements JTAG Technologies has devised a number of different programming mechanisms that are summarised as follows:-

### 'Ready to Run' (R2R).

Devices supported by this system use the low-level (BSX) application files supporting erase/program/verify etc.. that have been carefully prepared to support the non-

standard behavior of each device type. Thanks to the flexibility of the BSX code both JTAG and similar non-JTAG interface parts are supported by R2R files. In the case of non-JTAG parts a hardware adapter (SCIL module) is often required.

### 'ProVision Modelled' (PVM).

All standard NOR flash and many SPROMs are supported by ProVision models that will generate Erase, Program, Verify type routines.

Many Micro-Chip PIC devices can be programmed using PVM. Often it is convenient to access the PIC programming signals via a JTAG DIOS module that can be added into the interface pod itself.

Other mechanisms. Some parts are supported by special-to-type (STT) APL syntax files, SVF syntax files or modified IEEE Std 1532 format files.

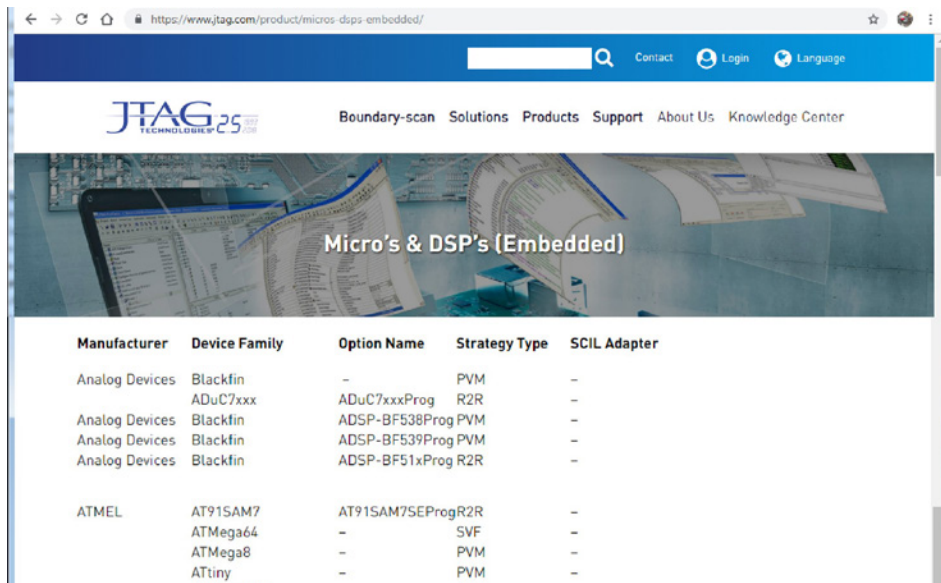
## Programming options

R2R:	Factory prepared files for high-speed
PVM:	ProVision Model supported.
STT:	Custom prepared APL, or SVF file

# SCIP - SERIAL CONTROLLED IC PROGRAMMING

Solutions for programming  $\mu$ Processors,  $\mu$ Controllers, DSPs with embedded flash

<https://www.jtag.com/product/micros-dsps-embedded/>



## SCIL Hardware Options



JT 5112 64 Channel MIOS



JT 5705/FXT Controller/MIOS



JT 2149 DIOS for QuadPod



JT 5705/USB Controller/MIOS

Region or Country	Telephone	E-mail
• USA and Canada	Toll free - 877 FOR JTAG Western US - 949 454 9040	info@jtag.com
• Europe and Rest of World	+31 (0)40 295 0870	info@jtag.nl
• Finland	+358 (0)9 4730 2670	finland@jtag.com
• Germany	+49 (0)971 6991064	germany@jtag.com
• Sweden	+46 (0)8 754 6200	sweden@jtag.com
• United Kingdom and Ireland	+44 (0)1234 831212	sales@jtag.co.uk
• China, (Malaysia, Singapore, Thailand, Taiwan, South Korea)	+86 (021) 5831 1577	info@jtag.com.cn
• Russian Federation	+7-(812) 3139159	Russia@jtag.com

1509 SCIP\_E  
© 2019 The JTAG Technologies logo and other trademarks designed with the symbol "®" are trademarks of JTAG Technologies registered in Europe and/or other countries. JTAG Technologies reserves the right to change design and specifications without notice.

