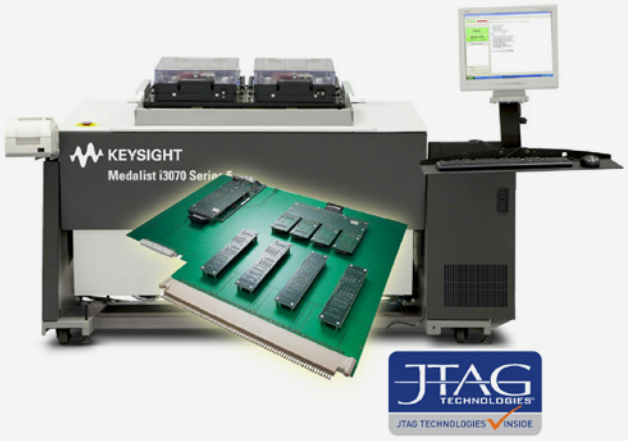
Factsheet

JTAG TECHNOLOGIES SYMPHONY INTEGRATION SOLUTION KEYSIGHT 3070

Boundary-scan solution for In-Circuit Tester



Keysight 3070 Symphony Highlights

- Integration solution for Keysight and JTAG Technologies
- Supports all 3070 series
- Fast integration of the boundary-scan hardware direct into the ICT's 'Test Head'
- Easy test program creation and debugging using JTAG Technologies' ProVision™
- Dedicated, Keysight-comptaible hardware
- Supports test and in-syem programming applications of JTAG/non-JTAG devices
- Offers an increase in test coverage while reducing adaptor costs
- Windows and HP-UX (Unix) platforms supported

The impact of modern designs

Increasing functionality, alongside miniaturization of components, dictates the use of leading edge component technologies such as Ball-Grid Arrays (BGAs) and Chip-Scale Packages (CSP). The net effect is a significant reduction in the number of physical access points. This in turn results in reduced test coverage for established testing processes such as In Circuit Test or Flying Probe Test. Even when it is possible to probe all required test points, the large number of pins in the ICT fixture and their reduced sized, simultaneously increases cost and reduces fixture reliablity.

The solution approach

Symphony series of integration solutions by JTAG Technologies makes it possible for users to continue getting the most out of their existing test systems.They provide increased fault coverage and improved diagnostics, while reducing costs for complex designs.

The Symphony 3070 package was developed to allow offline development and debug of test and ISP applications in JTAG ProVision™ that can be easily ported for integration in a 3070 'Test Plan'.
A customized version of the JT 37x7 controller - The JT 37x7/APC - is included in the package and fits into one of the 3070 pin-card slots, providing all TAP and IO resources via a standard 'MINT' connector. Connection to the 3070 controller via USB or Ethernet allows support for legacy HP-UX systems as well as Windows. In the JT 37x7/APC all TAP signals are also relay-isolated from the system to help prevent interference and unwanted ground loops.

Image 1, shows a 3070 ICT next to the custom JT 37x7/APC JTAG Controller including QuadPod and isolation relays.

Supported Systems:
Keysight 3070 series

The Symphony 3070 Package at a glance:
Hardware
- JT 37x7/APC JTAG Controller (custom for 3070) with isolation relays

Software
- JTAG Technologies software for performing boundary-scan tests and in-system-programming
- Boundary-scan-diagnostics for error analysis at pin level and transfer to the ICT System
- Windows or HP-UX versions
- Permanent node locked license including Sentinel USB Key for Windows controllers - hostid locked for HP-UX.

ISP and SCIL support

A valued feature of JTAG Technologies Symphony is the wide-ranging In-System (device) Programming

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support. As well as the estabished support for JTAG-direct programming of CPLDs and FPGAs plus indirect programming of flash devices Symphony 3070 can support programming of 'device embedded' memories. Such memories are typically, but not exclusively part of a processor or SOC. Usually programming access is provided by the JTAG interface and a standard TAP pod can be used. However in some cases a ISP-specific bus protocol is needed and these can be provided by JTAG Technologies' Scan-Controlled Interface Logic (SCIL) modules. SCIL modules replace standard TAP pods in the JT 37x7/APC. This feature can further simplify test set-ups by removing the need for dedicated 'in-fixture' programmers.

Furthermore, the solution supports the JTAG Core-Commander module for microcontrollers and FPGAs for embedded testing and programming solutions.

Example 3070 Test Plan Routines

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Keysight 3070  TestPlan summary of sub-routines for JTAG execution

☐ Sub Jtag -  operates TAP isolation relays and prepares system for application
  execution

☐ Sub  JtagTest(TestName$) - called from sub Jtag executes test with name
  TestName$.bat

☐ Sub ProcessJtagFailure(TestName$) - called if variable JTAG_BSD is set and runs
  diagnostics, adding output to the error report.

☐ Sub JtagFlash (Dev$) - executes and flash program applications for device instance
  (Dev$)

☐ Sub ProcessCluster(TestName$) - generates additional pin/node information for failed
  (logic) cluster tests
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