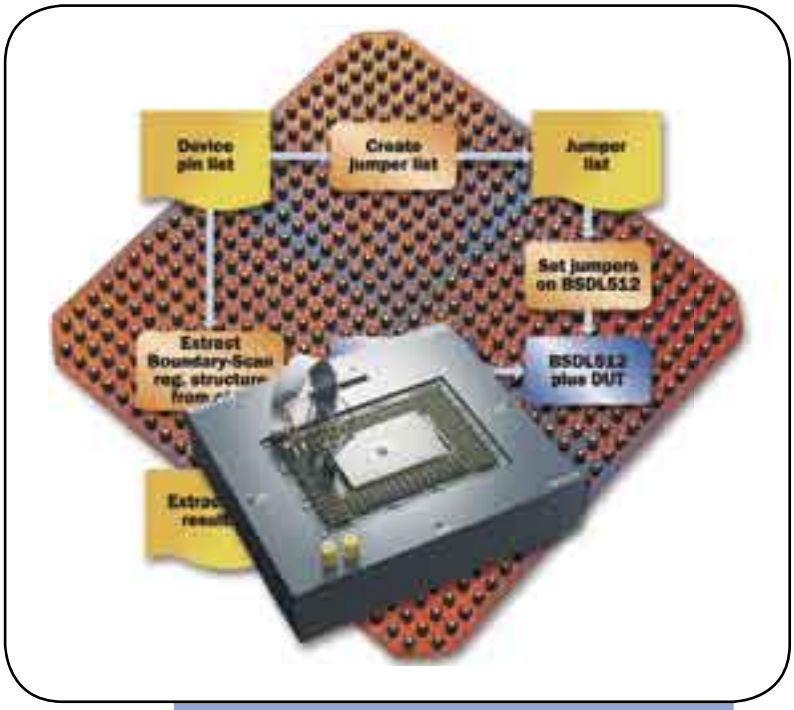
BSDL Generation/Verification System

Automated generator and verifier for boundary-scan description files

Features



- Easy-to-use software and hardware create and verify Boundary-Scan Description Language (BSDL) files using the actual integrated circuit
- Wizard guides the user through the generation / verification process
- Graphical editor provides interactive preparation of pin list for PGA and BGA device packages (in case no BSDL file exists)
- Table-structured editor generates pin list definition interactively for other device package types (in case no BSDL file exists)
- Extensive reporting features: cell list, pin list, input list, output list, register information
- Support for wide range of package types: PGA, BGA, QFP, TSOP, etc. with automatic wiring/netlist generation software
- 512 I/O channels each with independent sense, drive, bi-directional, and tri-state capabilities
- 1, 2, 4, or 8 I/Os selectable per segment of 16 I/Os
- Input and output voltage levels separately programmable per segment and segments can be individually bypassed
- Programmable input threshold from 0 V to 4.1 V in steps of 0.1 V
- Programmable output voltage from 1.5 V to 3.6 V in steps of 0.1 V
- Internal 5 V power supply plus three flexible power supply points
- High-speed TCK (up to 40 MHz) for maximum performance
- Hot Swap: target device may be connected and disconnected between tests without switching power off
- Fully compatible with JTAG/IEEE 1149.1 boundary-scan standard

General Description

Using an actual boundary-scan IC, the JTAG Technologies BSDL Generation / Verification System automatically verifies the existing BSDL file or creates a BSDL file for the device if none exists, all in accordance with the IEEE 1149.1 Boundary-scan Standard.

A BSDL file describes the boundary-scan characteristics of a specific device in terms of scan register lengths, ID codes, instruction codes, etc. Having correct BSDL files that correspond precisely to the design as implemented in the devices is a pre-requisite for developing safe boundary-scan applications at the board level. Therefore, the BSDL Generation / Verification System is a valuable tool for engineering and quality organizations of IC vendors, for ASIC design groups, and for test engineering departments.

JTAG TECHNOLOGIES™

Functional Description

The BSDL System consists of BSDL generation / verification software, BSDL512 hardware unit and the JT 3707 boundary-scan controller. The BSDL System automatically extracts the boundary-scan register structure from a sample of the IC and verifies it for compliance with the IEEE 1149.1 boundary-scan standard and for agreement with the description in an existing BSDL file. If there is no existing BSDL file, the system automatically creates it from the device.

The verification and generation processes start with preparation of the device pin list (see Figure 1) which provides information about the pin type: PWR, GND, signal, TAP, NC, etc. If a BSDL file is already available, then the device pin list is automatically extracted from the BSDL file. Otherwise, the Pin List Editor is used to create the pin list, graphically for PGA and BGA device packages and with a tabular structure for other types of device packages.

Before starting the extraction process using the hardware, the hardware configuration of the system is set up to match the chip pin-outs and voltage levels. Matching is easily accomplished by the jumper list that is automatically generated from the device pin list (See Figure 2).

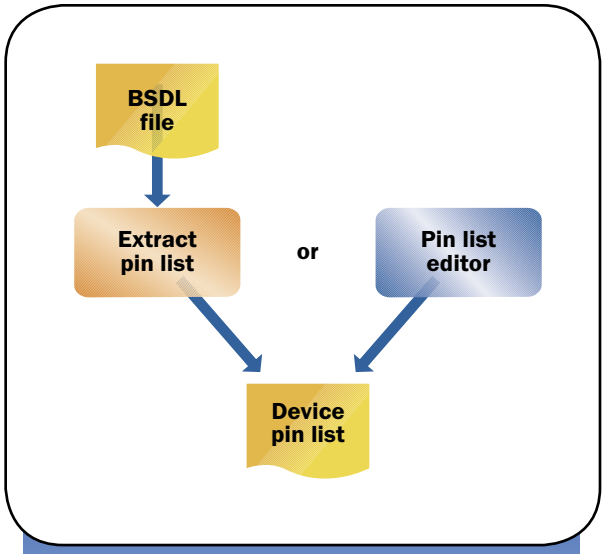


Fig. 1. Creating Device Pin List

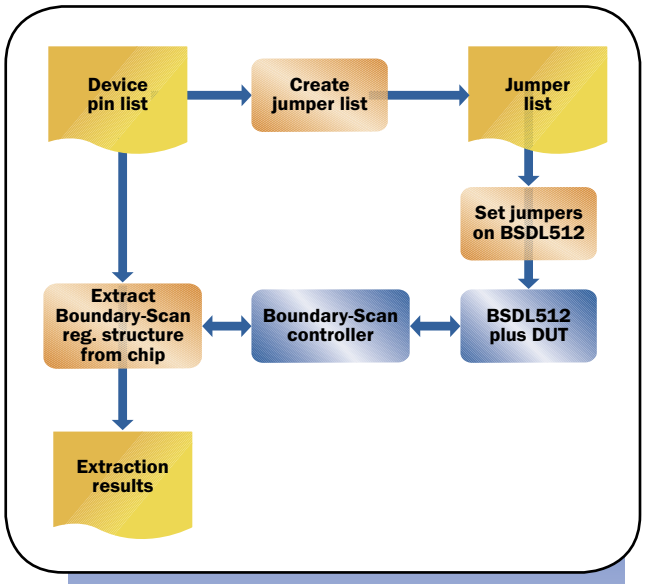


Fig. 2. BSDL Generation and Verification Process

Using the results from the extraction process, in the case where a BSDL does not already exist, the system generates the BSDL containing:

- pin_map and its attributes
- EXTEST and BYPASS instruction definition
- boundary-scan register description

If a BSDL file exists, then the extraction process produces a verification report which contains the cell list, pin list, input list, output list and register information. Also the ID code, if present, is verified.

The hardware of the BSDL Generation / Verification System – BSDL512 - supports 512 functional I/O channels. Each channel may be independently set to function as an input, output, bi-directional, or tri-stated signal. To match current IC technologies, the I/O channels support programmable input thresholds from 0 V to 4.1 V in steps of 0.1 V and programmable output voltages from 1.5 V to 3.6 V, also in steps of 0.1 V. The connection between the BSDL512 and the target IC is realized by means of an IC adapter board.

The adapter board connects to the system via an inner ring of connectors. IC adapter boards for BGA, QFP, TSOP, PLCC, and PGA devices are available in solder-on and socketed versions. Each adapter supports a specific device package type and pin-count or range of pin-counts. See Figure 3 for examples of the IC Adapter Boards. Please contact JTAG Technologies for information on other adapters for your specific applications.

I/O channel access is also provided to an outer ring of pins so that all pins can be easily accessed for manipulation or measurement. This usage of the outer ring of pins is shown in Figure 4.

Users can connect up to four different power supply levels on the IC pins to meet device requirements. One of the voltage levels, 5 V, is provided internally, and the other three are provided externally by the user. Also, a board is provided to check continuity and confirm proper operation of the unit.

Fig. 3. Examples of Adapter Boards

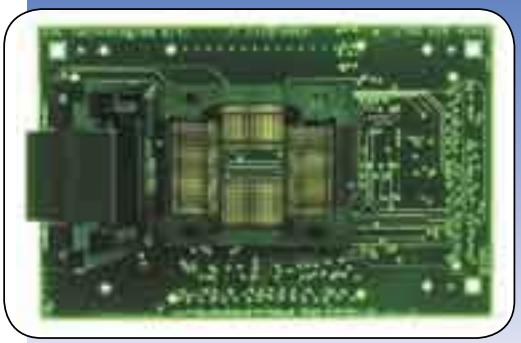


Fig. 4. Use of Outer Ring with the IC Adapter Board

Available Solder-on Adapter Boards

BGA144 (1.0 mm pitch, 12 x 12 grid)	QFP132, 196 (0.025" pitch)
BGA400 (0.8 mm pitch, 20 x 20 grid)	QFP144, 208 (0.5 mm pitch)
BGA400 (1.0 mm pitch, 20 x 20 grid)	QFP168, 184 (0.65 mm pitch)
BGA400 (1.27 mm pitch, 20 x 20 grid)	QFP32, 44, 128 (0.8 mm pitch)
BGA484 (1.0 mm pitch, 22 x 22 grid)	QFP48, 80, 160, 176 (0.5 mm pitch)
LQFP120, 128, 176 (0.4 mm pitch)	QFP48, 60, 136 (0.8 mm pitch)
PGA169 (0.1" pitch, 13 x 13 grid)	QFP52, 80, 240 (0.65 mm pitch)
PGA225 (0.1" pitch, 15 x 15 grid)	QFP56, 64, 136, 144 (0.65 mm pitch)
PGA289 (0.1" pitch, 17 x 17 grid)	QFP56R, 80R (0.8 mm pitch)
PLCC 20, 28, 32, 44, 52, 68, 84, 100, 124 (1.27 mm pitch)	QFP64, 304 (0.5 mm pitch)
QFP 84, 100 (0.025" pitch)	QFP64,120 (0.8 mm pitch)
QFP100, 240 (0.5 mm pitch)	QFP68, 164 (0.025" pitch)
QFP100R, 160 (0.65 mm pitch)	QFP84,120 (0.8 mm pitch)
QFP112, 232 (0.65 mm pitch)	TSOP28, 32, 40, 48 (0.5 mm pitch, 20 mm wide)
QFP120, 216 (0.5 mm pitch)	TSOP32, 40, 48, 56 (0.5 mm pitch, 13.4, 14, 18mm wide)
QFP128R, 256R (0.5 mm pitch)	

Available Socketed Adapter Boards

BGA361 (1.27 mm pitch, 19 x 19 grid), BCP361-1290-19AA11	QFP208 (0.5 mm pitch), IC201-2084-001 & IC201-2084-029
BGA372 (1.27 mm pitch, 20 x 20 grid), NP276-37206	QFP240 (0.5 mm pitch), IC51-2404-1655-2
PLCC 20, 28, 32, 44, 52, 68, 84 (1.27 mm pitch)	QFP64 (0.5 mm pitch), IC201-0644-003
QFP160 (0.65 mm pitch), IC51-1604-845-4	

For other types, please contact JTAG Technologies.

BSDL Generation/Verification System

Hardware Specifications

Input thresholds	Programmable from 0 V to 4.1 V in steps of 0.1 V per segment of 16 I/Os
Output voltages	Programmable from 1.5 V to 3.6 V in steps of 0.1 V per segment of 16 I/Os
Power supply	0.9 V to 5.5 V, 50 to 500 mA max
I/O channels	Input, output, bi-directional, tri-state output (8 segments, 16 I/O per segment)

Ordering Information

Part Number	Description
BSDL 512 System	BDSL Verifier and Generation software including automatic adapter wiring generation software, BSDL512 verifier hardware supporting up to 512 I/O channels and JT 3707 DataBlaster boundary-scan controller
JT 2125/<package_type>	IC Adapter Board for <package_type> (socketed)
JT 2126/<package_type>	IC Adapter Board for <package_type> (solder-on)

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