

# JT 3705/USB - 'EXPLORER' 2 TAP CONTROLLER

Portable JTAG/boundary-scan controller for test and programming PCBAs



## Key features

- Two independent TAPs (Test Access Ports) for flexible board interfacing
- Fully Compatible with IEEE 1149.1, IEEE 1149.6, IEEE 1149.4 and IEEE 1532 standards
- Fully programmable voltage TAP (1.5V to 3.6V)
- Up to 6MHz programmable TCK frequency
- USB Powered (no external PSU needed)
- For boundary-scan /JTAG testing PLD & FPGA downloads and small-scale flash programming
- JTAG ProVision™ compatible
- Stylish contemporary design

## Introduction

To address the steady growth of JTAG/boundary-scan (IEEE Std 1149.1) devices in electronic designs. JTAG Technologies has developed the only truly low-cost, fully functional boundary-scan controller featuring two test access ports (TAPs). The market for boundary-scan tools has evolved greatly throughout the 21st century and JTAG/boundary-scan logic is now fitted as standard to all CPLD's and most 'processors.

## Multiple TAPs

The new JT 3705/USB is USB powered, making it easily portable. Its two TAPs can be fully synchronised for test purposes and it is compatible with all JTAG Technologies' developer tools such as JTAG ProVision and JTAG Live. Within ProVision multiple JT 3705s can be 'linked' to provide even higher TAP counts. The JT 3705/USB can be used equally for structural board testing or in-system device programming (ISP) of CPLDs flash memories etc..

## Programmable levels

Programmable output levels per TAP (1.5V to 3.6V) make the JT3705/USB compatible with all current and future logic families. Test clock frequency may also be programmed from 1KHz to a brisk 6MHz allowing test applications to be executed in a 'snap'.

## Software options

With a JT 3705/USB and a basic ProVision Platform set-up SMEs can equip themselves with an affordable yet potent structural test system. Alternatively team the JT 3705/USB with Python-based JTAGLive Script or Studio for a powerful JTAG functional test system.

This product represents a significant breakthrough and puts boundary-scan test within reach of many more would-be users.

## Ordering information

JT 3705/USB - Explorer - fast two TAP boundary-scan controller/ programmer.

# JT 3705/USB - 'EXPLORER' 2 TAP CONTROLLER

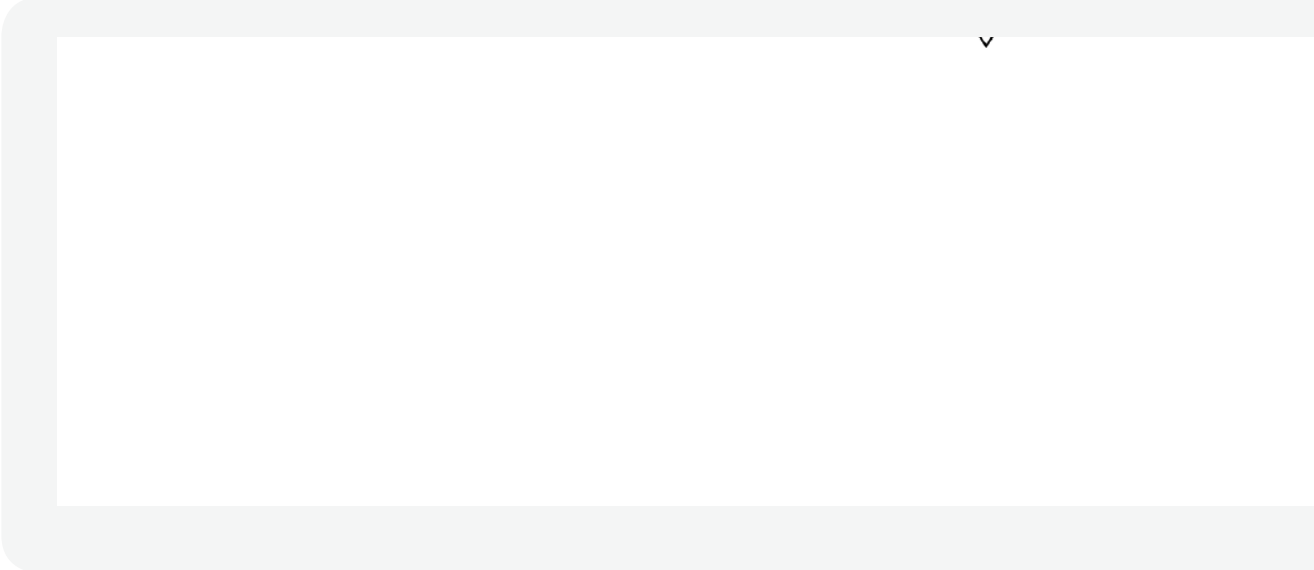
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The image displays a logic analyzer interface with two main windows. The top window shows a netlist with signals such as ADDRESS0 through ADDRESS15, DATA, and various control signals. The bottom window shows a Verilog HDL code editor with the following code:

```

1 Model for F_LQTH M29F010
2 nmk: m29f010 (A10 not used)
3 Created on March 5, 2009
4 Mod.Filed April 2, 2009
5
6 @author: JTAG Technologies
7
8
9
10
11 from jt import *
12 import time
13
14 DeclareGroup("ADDRESS", ["A15","A14","A13","A12","A11","A10","A9","A8",
15 "A7","A6","A5","A4","A3","A2","A1","A0"])
16
17 DeclareGroup("DATA", ["DQ17","DQ16","DQ15","DQ14","DQ13","DQ12","DQ11","DQ10"])
18
19 HOLD_TIME = 0.01 #10 ns
20
21 SetMode(1) #Immediate Access at initialization time
22
23 def WriteData(a):
24     t["w"] =
25     t["d"] = a
26     t["a"] = ADDRESS
27     t["m"] = "w"
28     t["n"] = "a"
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```

## TAP connections



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