Why test?

By Peter van den Eijnden

Design for Manufacturing (DFM) rules and highly automated assembly equipment minimize the number of assembly errors on your printed circuit board assemblies (PCBAs). To deliver fault free, high quality PCBAs they must be tested to detect and remove any remaining assembly errors. Detection of such errors as early as possible, i.e. at board level before system level assembly, is crucial to save costs.

The amount of money that will be spent on testing in manufacturing (the recurring costs) and in field service is determined by the testability of the design and hence is committed during the design phase of the product. The relationship is shown in the figure below.

If during the design phase no attention is paid to testing at all, then it should come as no surprise that testing the board in manufacturing can be very expensive. Maybe certain nodes cannot be controlled independently by the tester (eg a reset pin directly tied to Vcc or ground) or the possibility to find the cause of a fault - the fault diagnosis - may get very complex.

Miniaturization and increasing device complexity
Smaller device packages and increasing device complexity limit the test coverage and diagnostic capabilities of traditional test methods like in-circuit test (ICT), flying probe test (FPT) and functional test (FCI). JTAG test and in-system programming applications use the resources built into the chips on your boards and are complimentary to the traditional test methods.

Combining JTAG with traditional test methods results in higher test coverage for all types of boards.

JTAG boundary-scan added to an ICT/FPT specifically helps to restore test access. JTAG boundary-scan added to a functional test systems helps to detect and diagnose manufacturing defects more easily. Also it can help to more easily create specific starting states for the functional test on a board, or to inspect signal states at any point during the functional test.

DFT rules
Using the latest test technologies and applying Design for Test (DFT) rules results in boards that are better testable and helps to minimize the costs of testing in production.

The JTAG interface on many of today’s devices provides an excellent opportunity to limit the recurring test costs of a printed circuit board.

Through this interface test and in-system programming on a board is possible using the resources built into the chips on a board. By taking a few simple Design for Test (DFT) rules into account different JTAG test and programming applications can easily be created, and can be used efficiently in manufacturing as well as field service. A complete overview of Design for Test rules at board and system level can be found in JTAG Technologies’ DFT booklets. Both are available for free through our website: www.jtag.com.

Check testability and fault coverage
When JTAG testing is used you can calculate the testability of your design. A product like JTAG ProVision includes integrated testability and fault coverage analysis with details of the net and pin-level testability. If your testability goals are not met, you can correct your design as it progresses, right on your schematic and layout drawings.

Comparing the total coverage of the created applications against the calculated testability of the board quickly reveals if additional tests need to be developed. Closely watching the testability of your design and fault coverage of your tests not only limits the test costs, but also helps to get products to market faster with higher quality levels.

JTAG for testing and in-system programming for prototypes and small production series
JTAG test and in-system programming use the resources (boundary-scan registers, debug registers, etc.) built into the chips on your boards. These embedded resources can be accessed with a simple JTAG controller that interfaces your PC with the JTAG interface on your board. For higher demands advanced, high performance JTAG controllers are available.

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in higher volume production, similarly the analog circuitry is handled by the ICT or FPT. To handle the analog circuitry of a board in a stand-alone system Mixed-Signal I/O capabilities are available with JTAG Technologies’ boundary-scan systems (JTAG controllers, I/O modules and software).

**Background on JTAG boundary-scan**

With boundary-scan a shift register is added in silicon along the pins (the boundary) of the chip. With each (digital) pin of the chip one or more cells of this shift register are associated. Through these cells one can now control and observe a device pin independent of the functionality (core logic) of the chip. The connection between the pins of two, or more boundary-scan chips can easily be verified. All it takes is to drive a 0/1 on an output pin via its bit in the bscan reg and then observe the value seen by the connected input pin(s) via their bits in the bscan reg’s of the chips.

This forms the basis of boundary-scan.

In this way the connections between bscan devices can easily be verified, even if other non-bscan devices are in between. A very simple example of such device would be a series resistor.

When bscan devices are connected to the address, data and control pins of a flash memory then this memory can be written to and read from via the bscan registers of these devices. In this way in-system programming of flash memories via JTAG is possible.

Microprocessors often contain special JTAG accessible debug logic for software debugging purposes. This logic may be in addition to a boundary-scan register in the chip. Sometimes, however, a boundary-scan register is not present in those chips. Through the debug logic one has full JTAG control over the CPU core and its busses and everything connected to it. This debug logic can now be used for test and in-system programming purposes (emulative test and programming).

JTAG Technologies’ CoreCommanders interface directly with the debug logic of a microprocessor and provide full control over a processor core. CoreCommanders are specific for a processor core, a processor type, or processor family. The functions of a CoreCommander – its API – are independent of the type of processor core.

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The applications, debugging, testing, in-system programming of programmable logic (FPGAs and cPIDs) or flash memories, etc. are determined by the software being used. For basic testing buzzing-out connections interactively and interactive verification of a cluster (i.e. a non-boundary scan device surrounded by boundary-scan devices) may already be sufficient. More functionality and automation, e.g. automatically generate various JTAG boundary-scan applications, run a sequence of test and in-system programming actions, etc. can simply be added by further software modules.

A simple controller plus some interactive test capabilities in addition to your normal functional test set-up may be sufficient for debugging and testing prototypes as well as small production series. The JTAG controller plus test and in-system programming software can be used stand-alone, or be integrated with your functional test set-up: “JTAG Technologies inside”.

You can thus scale your JTAG test and in-system programming solution from a simple controller with some basic test software all the way to a fully equipped system with automatic application generators and advanced sequencing capabilities. This makes JTAG a cost-effective approach not only for higher volume production, but also for prototype testing and small volume production.

Even if only one device on the printed circuit board assembly (PCBA) has boundary-scan JTAG testing can already be used. The more JTAG access is available on a board the higher the fault coverage via JTAG. The amount of JTAG access on a board not only depends on the number of boundary-scan devices that is present, but also which device types have boundary-scan. If in a CPU-centric or FPGA-centric design only the CPU or the FPGA has boundary-scan and/or a JTAG debug register the fault coverage via JTAG can already be very high.

**Covering analog and digital**

Boards contain a mix of analog and digital circuitry. JTAG boundary-scan is mostly limited to digital signals (although an analog boundary-scan standard does exist). When JTAG is combined with functional testing the analog signals are often handled by the analog instruments used for the functional tests. When JTAG is combined with ICT and FPT systems, often used