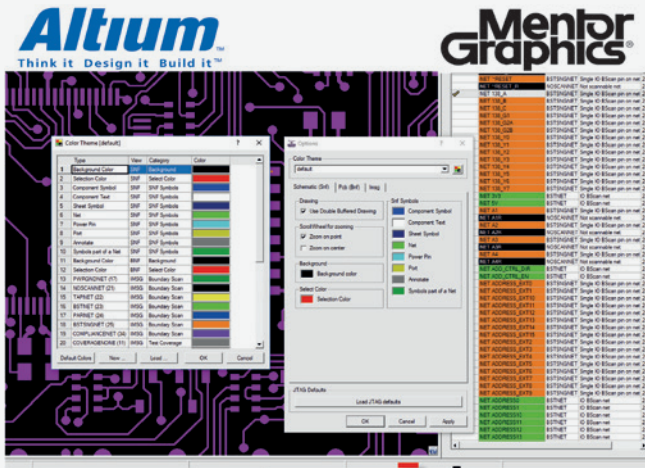


# JTAG VISUALIZER FOR DFT AND FAULT ANALYSIS

## Interactive Schematic and Layout Viewers



- Rapid view of the JTAG access and testability of your design through schematic or layout displays
- Maps feature assists DfT and exports ProVision archive
- Maps feature checks BSDL models semantics/syntax
- Enables speedy fault location
- Displays learned scan-chain
- Use as a stand-alone system, a ProVision plug-in or custom run-time set-up (Active-X)
- Extensive search and display features: locate, zoom to, next node
- Compatible with all leading EDA tools
- Multiple language options - German, French, Russian, Japanese and Chinese

### Introduction

JTAG Visualizer is a design data viewer that also integrates with JTAG Technologies' family of boundary-scan products and selected 3rd party systems. JTAG Visualizer accepts input data (schematic, layout, and information files) from sources such as EDA tools enabling faster DfT analysis and fault finding on boundary-scan target designs.

### Applications

JTAG Visualizer enhances the power of boundary-scan throughout board design, manufacturing and repair. Locating specific nets, components and other items in the schematics or layouts is a snap - even for the most complex designs. And, while a designer may wish to check schematics and/or layouts for (boundary-scan) testability, production and repair technicians will benefit from faster graphical location of diagnosed faults on layout.

### Highlighting the schematics

During design, an important task is to assure 'testability', a process often referred to as Design-for-Test, or DfT. The life-cycle benefits of boundary-scan are greatly enhanced by a formal approach to DfT prior to committing the design to layout. ProVision users with JTAG Visualizer, can easily view the parts of the schematic defined as testable and which parts need improvement. This is achieved by combining the schematic

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### Ordering information

- JTVB - JTAG Visualizer for Board Layout - includes one CAD extractor/converter
- JTVS - JTAG Visualizer for Schematics - includes one CAD extractor/converter Prerequisites Software
- ProVision V2.0 or PSA or PIP/\*\*\*. BSD Diagnostics recommended with layout viewer

### Supported Schematic Systems

- Altium - Designer
- Cadence - OrCAD Capture, Concept
- Mentor - CAMCAD, DxDesigner [EE 7.9.3 + and ViewDraw], Design Capture 2002/2004, Design Architect, PadsLogic 2005/2007
- Zuken - CR5000, CadStar

### Supported Layout Systems

- Valor ODB++, ODBXML
- Altium P-CAD, Designer
- Cadence Allegro
- Fabmaster FATF
- Mentor - CAMCAD, PADS PowerPCB, PADS Layout, BoardStation, Expedition PCB
- DDE-EDA - Supermax ECAD
- Intercept - Pantheon
- Zuken CR5000, Cadif

data with actual test application data. Alternatively Visualizer's Maps feature offers a basic accessibility review from a simple mouse click. Customizable colors, indicating test coverage levels or access types can be displayed in a color-coded

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schematic. Once the design has been optimized for boundary-scan test and committed to layout, final application development can begin in the JTAG ProVision development environment.

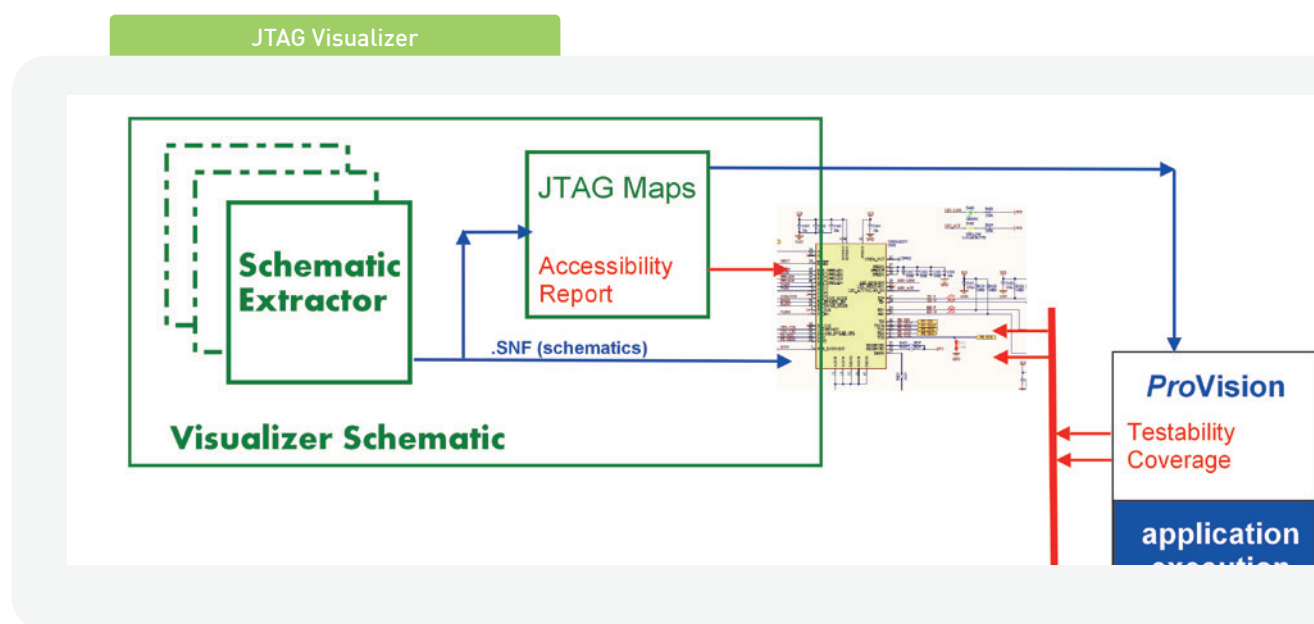
#### Manufacturing use

JTAG Visualizer greatly facilitates the repair of defective boards by showing the faults graphically in the layout and in the schematics. From ProVision Visualizer can be launched automatically using the 'Visualise nets on Fail' feature. Alternatively the output from JTAG's pin-level diagnostics reporter can be overlaid

onto Visualizer with the click of a mouse, allowing a technician to find all instances of the faulty net(s) within the physical layout or schematic circuit.

#### Advanced Features

Visualizers' flip feature allow an instant turn of the layout view to see how boards might look from the underside. Locate, Zoom to and Find next also help the user to navigate through the design. These features illuminate only selected nets and help to track these as they pass through multiple board layers.



Region or Country	Telephone	E-mail
• Europe or Rest of World	+31 (0)40 295 0870	info@jtag.nl
• United Kingdom & Ireland	+44 (0)1234 831212	sales@jtag.co.uk
• North America	Toll free - 877 FOR JTAG Western US - 949 454 9040	info@jtag.com
• China, Malaysia, Singapore, Thailand, Taiwan	+86 (021) 5831 1577	info@jtag.com.cn
• Germany	+49 (0)971 6991064	germany@jtag.com
• Finland	+358 (0)9 4730 2670	finland@jtag.com
• Sweden	+46 (0)8 754 6200	sweden@jtag.com

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