

CTPG_M - CORECOMMANDER TEST PROGRAM GENERATOR FOR MEMORIES

Automatic generator for at-speed test of memory clusters by debug logic embedded in FPGAs or microprocessors



- Speed-up memory testing
- Improve functional test
- Catch parasitic impedance faults
- Improve board test fault coverage
- Uses existing hardware and diagnostics software
- Based on tried and trusted memory cluster test algorithms

Introduction

At the heart of JTAG Technologies' Emulative Test & Programming (ETP) technology are the CoreCommanders that offer access to the emulation modes of μ processors or the internal IP bus of an FPGA. Within JTAG ProVision the CoreCommander options can be used interactively or to execute a sequence of commands - for example to test the connections to a memory device. With CTPG_M these tests can be generated automatically for testing both connectivity and functionality between the core host (μ processor or FPGA) and all kinds of memory devices including DDRx devices.

Using the device kernel

CTPG_M has been developed in-house to overcome many of the issues associated with testing of memory clusters using conventional boundary-scan (IEEE Std 1149.1) techniques. These issues can include the lack of a boundary-scan register (generally in smaller CPUs), insufficient access to all memory signals (most notably synchronous memory clocks) and also the inability to test using write/read cycles running at full system speed. By harnessing the power of the embedded emulation/debug logic and the embedded memory controller, tests can be developed automatically to overcome the issues listed above, allowing faster and more effective testing.

Order information
CTPG_M - CoreCommander Test Program Generator for Memories

As part of JTAG Technologies broader range of ETP products CTPG_M aims to increase both fault coverage and test throughput on compatible designs. The system utilises existing debug/emulation support options built-into microprocessors or downloaded into FPGAs covering most of the chips based on the popular ARM cores as well as cores from Analog Devices, Infineon, NXP (Freescale), ST Microelectronics, TI, Microchip and Marvell (Xscale), and parts from Altera and Xilinx.

Option for ProVision

CTPG_M is available now as an option to JTAG ProVision software from CD release 23. It is fully compatible with all JTAG Technologies tester hardware and diagnostics system enabling pin-level diagnostic reports to be produced for test engineers, production technicians et al. Test results can thus also be viewed in layout or schematic views provided by JTAG Technologies Visualizer tools.

Generation of a test requires you to identify the core on your target board together with the memory device to be tested. After providing the memory's start address CTPG_M will automatically generate the correct se-

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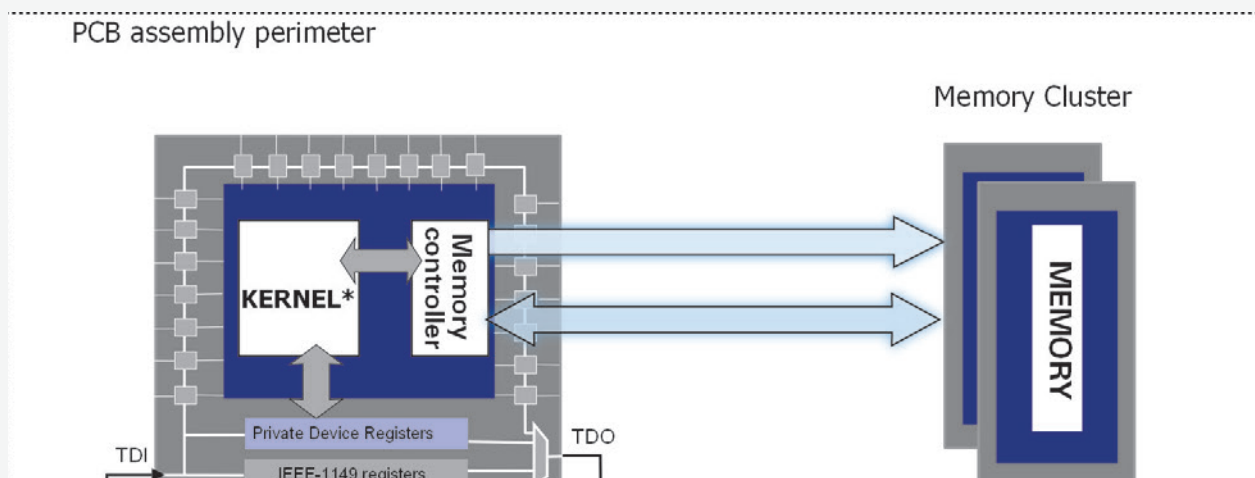
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quence of commands for the CoreCommander. Information on the type of memory to be tested is provided to CTPG_M in a standard ProVision model file. If an embedded memory controller is present CTPG_M reads the settings needed to set up the various aspects of the controller (e.g. INIT AIPS, INIT PLL, INIT DDR) from a target related initialization file.

Test Execution

During test execution at-speed writes and reads to the external memory are performed following an optimised test procedure developed by JTAG Technologies. In a similar manner to conventional (boundary-scan based) tests the results are displayed in the familiar truth-table format, prior to parsing by BSD diagnostics in the case of a test fail.

Figure 2



Block diagram of CTPG_M in action

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