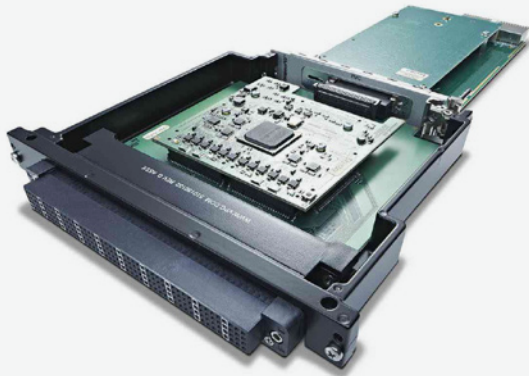


JT 2147/VPC- JTAG/BOUNDARY-SCAN INTERFACE SYSTEM

Custom signal-conditioning pod for Virginia Panel systems



JT2147/VPC Highlights

- High integrity interface for JTAG Technologies' 'DataBlaster' PXI(e) controllers
- Provides four JTAG Test Access Ports (TAPs)
- Includes up to 64 boundary-scan DIO lines
- Designed for connection with G20x or G14x 192 'QuadraPaddle' connectors
- Compatible with VPC 'pull-through' system
- Enables high-speed boundary-scan test & device programming applications
- Ideal for Mil-Aero and Telecoms functional test systems
- Preserves signal integrity right to the point of test

Product Overview

The JT 2147/VPC is a signal conditioning module that allows seamless connections from JTAG Technologies PXI & PXIe DataBlasters to the Virginia Panel mass interconnection system. Using the same technology as the widely used bench-top QuadPod from JTAG Technologies, the JT 2147/VPC has been specifically designed to interface to test fixtures using VPC's QuadraPaddle connector system. In using the JT 2147/VPC, test system builders will greatly simplify their wiring tasks and, at the same time, retain the excellent signal integrity assured by the QuadPod's active interface. The JT2147/VPC features four independent JTAG Test Access Ports (TAPs) along with 8 user assigned static DIO channels and 64 DIOS (boundary-scan synchronised DIO) channels. Each TAP can be programmed to operate through a range of voltage levels to suit various logic families.

SCIL Compatible

Two out of the four JTAG TAP 'slots' in the JT 2147/VPC can be reconfigured to support one of JTAG technologies SCIL (Scan Controlled Interface Logic) functions. SCIL functions include BDM programming protocol, I2C, ARM SWD and more - see separate SCIL datasheet for full details.

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Order Information

- JT 2147/VPC Virginia Panel QuadPod interface

Prerequisites

Hardware

- JT 37x7/PXI(e) DataBlaster

Software

- ProVision(Platform), Classic Developer, PSA or PIP

Specifications Brief

- Incorporates four IEEE Std. 1149.x test access ports
- Supports gang testing or synchronised across all 4 TAPs
- 40 MHz max TCK using internal reference clock
- Features AutoWrite™ for faster flash programming
- Output voltage 1.0V to 3.6V programmable per TAP
- Input threshold 0.5V to 1.8V programmable per TAP
- 16 'static' DIO lines (for relay switching etc...)
- 64 'dynamic' DIOS lines (for extended bscan testing)
- Direct connect to JT 37xx/PXI(e) controllers

JTAG/boundary-scan applications prepared using JTAG Technologies ProVision or 'Classic' software tools may be executed on this PXI platform with driver packages that are available for NI LabView, TestStand and LabWindows as well as Geotest ATEasy and a number of generic language compilers (e.g. .NET framework,

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C++, VisualBasic)

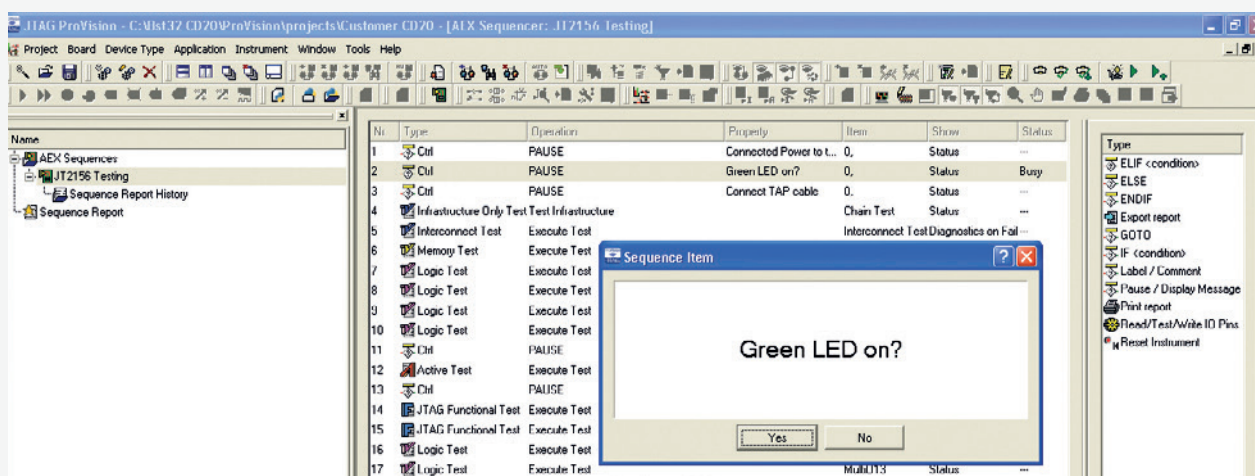
The boundary-scan application development tool - JTAG ProVision is capable of generating structural tests, functional mixed-signal tests, and device programming applications.

In most instances application development is a fully automated process using CAD data (netlist) and device models from JTAG Technologies' comprehensive

library and IEEE 1149.x compliant BSDL models from manufacturers of ICs. ProVision however also offers flexible customised programming options through its Python based JTAG Functional Test module.

Completed board test and device programming 'sets' can be invoked within a sequence through a wide choice of ATE environments such as Geotest (ATEasy), National Instruments (LabView (TestStand), Microsoft (C++ .NET) etc..

ProVision's Application Executive



Test sequencer & reporter

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