The Impact of High-Density PCB Design on In-Circuit Testing

As electronics designers continue to drive greater densities onto their printed circuit boards, testing for the occurrence of manufacturing faults becomes an increasingly difficult challenge for the test engineers. In-circuit testers can’t always guarantee adequate test coverage, because of the increased use of components with no physical access to the electrical pins: ball-grid array packages and inner board layers present inaccessible nodes, and the high density often makes the spacing between test points insufficient.

JTAG Technologies enables the SPEA 3030 testers to reach the greatest testability and programmability of complex PCBs, performing in-circuit and boundary-scan tests within a single process step.

Test Strategy Considerations

Choosing between the many possible combinations of inspection methods (for example, optical, X-ray, and boundary-scan) depends on several factors including the characteristics of the product to be tested, production throughput requirements, and the anticipated fault spectrum. Because boundary-scan and ICT are complementary test methodologies, this combination often provides an optimal test strategy with lowest overall cost and maximum coverage for anticipated fault types. One such valuable test platform is the JTAG Technologies Symphony SPEA3030™, combining the boundary-scan solution of JTAG Technologies with the SPEA 3030 in-circuit test system.

The JTAG Technologies Solutions

Symphony 3030 by JTAG Technologies is unique in its architecture, delivering the benefits of both boundary-scan and ICT without disrupting your existing test methodology. The JTAG Technologies test vector generation software ProVision, and the SPEA 3030 operating system Leonardo even use the same data since ProVision has direct access to information contained in the Leonardo board description.

Test and in-system programming applications are generated on JTAG Technologies development tools and easily ported to the 3030 system. There, the applications run on a high-performance JTAG Technologies controller delivering high throughput for in-system flash programming as well as testing applications.
Figure 2 illustrates the process flow, showing the JTAG Technologies applications running at the SPEA in-circuit tester, in a unique combined test system. The JTAG Technologies’ development tools support automatic generation of tests for the infrastructure, interconnections, memory cluster interconnections and clusters of non-scan devices as well as in-system programming of flash memory and CPLDs. Infrastructure test checks the integrity of the boundary-scan chain, verifying that the test resources are functioning properly before initiating subsequent tests. The interconnection test checks the connections between boundary-scan components, pointing out possible short circuits or pins not soldered. Test and in-system programming applications are executed on the JTAG Technologies boundary-scan controller, and its output is passed to the fixture via the JT 2147 QuadPod and TAP (Test Access Port) isolation modules mounted on the Spea64 direct interconnection unit.

- JTAG ProVision™
- JT 3727/TSI hardware controller/tester with QuadPod
- 4 off TAP isolators model JT 2139
- SPEA 64 direct access interconnection unit onto which JTAG QuadPod and 4 JTAG TAP isolators (JT2139) are mounted
- SPEA System Interface Block, for instruments and options
- JTAG Tester Interface Package: TIP SPEA3030 DLL
- Boundary-scan diagnostics for pin-level test failure analysis
- Node Locked license with a JTAG key
- User manuals

### Product Number | Description | Applications
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Symphony 3030 | Boundary-scan option for Spea 30301 ICTs | PCB Test, CPLD programming, and production flash programming in engineering

### Options
- JTVS, JTVB
  - JTAG Visualizer - graphical viewing tools for circuit schematics or PCB layouts

Fault coverage analysis during development, development, fault tracking in production/rework.

**SPEA requirements: System predisposition for JTAG boundary-scan installation (SPEA Code 45017432.114).**

### Ordering information:

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